CLAIMS

What is claimed is:

1. A method comprising:

extracting parameters of a set of domino logic circuits;

simulating each domino logic circuit of the set of domino logic circuits; and

reporting results of the simulating.

2. The method of claim 1 wherein:

each domino logic circuit having a set of inputs and an output and

simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated.

3. The method of claim 2 wherein:

simulating each domino logic circuit includes using the simulated results of circuits coupled to the inputs of the domino logic circuit.

4. A method comprising:

scheduling a set of domino logic circuits into an ordered list; and

simulating each domino logic circuit according to the ordered list.

5. The method of claim 4 further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits.

6. The method of claim 5 further comprising:

reporting results of the simulating.

7. The method of claim 6 wherein:

the scheduling includes scheduling the set of domino logic circuits such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino logic circuit.

8. The method of claim 7 wherein:

the extracting further including extracting parameters of non-domino circuits;

the scheduling further including scheduling non-domino circuits into the ordered list; and

the simulating further including simulating non-domino circuits.

9. The method of claim 8 wherein:

the reporting further including reporting results of the simulating non-domino circuits.

10. A machine readable medium embodying instructions which, when executed by a processor, cause the processor to perform a method, the method comprising:

scheduling a set of domino logic circuits into an ordered list; and

simulating each domino logic circuit according to the ordered list.

11. The machine readable medium of claim 10 further embodying instructions which, when executed by a processor, cause the processor to perform the method further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits.

12. The machine readable medium of claim 11 further embodying instructions which, when executed by a processor, cause the processor to perform the method further comprising:

reporting results of the simulating.

13. The machine readable medium of claim 12 further embodying instructions which, when executed by a processor, cause the processor to perform the method wherein:

the scheduling includes scheduling the set of domino logic circuits such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino logic circuit.

14. The machine readable medium of claim 13 further embodying instructions which, when executed by a processor, cause the processor to perform the method wherein:

the extracting further including extracting parameters of non-domino circuits;

the scheduling further including scheduling non-domino circuits into the ordered list; and

the simulating further including simulating non-domino circuits.

15. A system comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller;

wherein the processor executes instructions to perform the method of:

scheduling a set of domino logic circuits into an ordered list; and

simulating each domino logic circuit according to the ordered list.

16. The system of claim 15 wherein the processor further executes instructions to perform the method further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits; and

reporting results of the simulating.

17. An apparatus comprising:

means for extracting parameters for each domino logic circuit of a set of domino logic circuits;

means for scheduling the set of domino logic circuits into an ordered list;

means for simulating each domino logic circuit according to the ordered list

means for reporting results of the means for simulating.